Claims

[c1] A method of forming an isolation structure comprising:

(a) providing a semiconductor substrate;

(b) forming a buried N-doped region in said substrate;

(c) forming a vertical trench in said substrate, said trench extending into said N-doped region;

(d) removing said N-doped region to form a lateral trench communicating with and extending perpendicular to said vertical trench; and

(e) at least partially filling said lateral trench and filling said vertical trench with one or more insulating materials.

[c2] The method of claim 1, wherein step (e) comprises, in the order recited:

(i) partially filling said vertical and lateral trenches with a first insulating material;

(ii) removing said first insulating material from said vertical trench;

(iii) filling unfilled portions of said lateral trench and refilling said vertical trench with said first insulating material;

(iv) removing said first insulating material from said vertical trench; and

(v) refilling said vertical trench with a second insulating material.

[c3] The method of claim 2, further including annealing said first insulating material in an inert atmosphere after steps (i), (iii) and annealing said first and second insulating material in an inert atmosphere after step (v).

[c4] The method of claim 2, wherein said first and second insulating materials are independently selected from the group consisting of Silizane, TEOS and HDP oxide.

[c5] The method of claim 2, wherein said first insulating material is spun applied in steps (i) and (iii).

[c6] The method of claim 1 wherein step (e) comprises in the order recited:
(i) partially filling said vertical and lateral trenches with a first insulating material; and
(ii) completely filling said vertical and lateral trenches with a second insulating material.

[c7] The method of claim 6, wherein said first and second insulating materials are independently selected from the group consisting of TEOS and HDP oxide.

[c8] The method of claim 1, further comprising:
before step (e), forming an insulating liner on all exposed surfaces of said vertical and lateral trenches.

[c9] The method of claim 1, further comprising:

before step (b), forming an epitaxial silicon layer on said substrate.

[c10] The method of claim 1, wherein said substrate is intrinsic or P-doped to a maximum concentration of 1E17 atm/cm^3 and said buried N-doped region are formed by ion implantation of an N-type dopant ion with a dose of 1E14 to 1E16 atm/cm^2.

[c11] The method of claim 1, wherein said buried N-doped region are formed by ion implantation of arsenic, phosphorous or antimony or combinations thereof.

[c12] The method of claim 1, wherein steps (c) and (d) are independently performed using one or more plasma etch processes.

[c13] The method claim 1, further comprising:
forming an N-well or a P-well region in said substrate, said N-well or P-well partially bounded by said lateral trench; and
respectively forming the source and drain of an NFET or a PFET in said N-well or said P-well.

[c14] A method of forming an isolation structure comprising:
(a) forming a first patterned masking layer on a semiconductor substrate, whereby a portion of said substrate is exposed through an opening in said first masking layer;
(b) implanting ions into the exposed portion of said substrate thereby forming a buried N-doped region in said substrate;

(c) removing said first patterned masking layer and forming a second patterned masking layer on said substrate, an opening in said second masking layer aligning over a less than whole portion of said buried N-doped region;

(d) etching a vertical trench in said substrate through said opening in said masking layer, said trench extending into said N-doped region;

(e) laterally etching said N-doped region to form a lateral trench communicating with and extending perpendicular to said vertical trench; and

(f) at least partially filling said lateral trench and filling vertical trench with one or more insulating materials.

[c15] The method of claim 14, wherein step (f) comprises, in the order recited:

(i) partially filling said vertical and lateral trenches with a first insulating material;

(ii) removing said first insulating material from said vertical trench;

(iii) filling unfilled portions of said lateral trench and refilling said vertical trench with said first insulating material;

(iv) removing said first insulating material from said vertical trench; and

(v) refilling said vertical trench with a second insulating material.

[c16] The method of claim 15, further including annealing said first insulating material in an inert atmosphere after steps (i) and (iii) and annealing said first and said second insulating material in an inert atmosphere after step (v).

[c17] The method of claim 15, wherein said first and second insulating material are independently selected from the group consisting of Spin-On-Glass, TEOS and HDP oxide.

[c18] The method of claim 15, wherein said first insulating material is spun applied in steps (i) and (iii).

[c19] The method of claim 14 wherein step (f) comprises in the order recited:
(i) partially filling said vertical and lateral trenches with a first insulating material; and
(ii) completely filling said vertical and lateral trenches with a second insulating material.

[c20] The method of claim 19, wherein said first and second insulating materials are independently selected from the group consisting of TEOS and HDP oxide.

[c21] The method of claim 14, further comprising:
before step (f), forming an insulating liner on all exposed surfaces of said vertical and lateral trenches.

[c22] The method of claim 14, further comprising:

before step (b), forming an epitaxial silicon layer on said substrate.

[c23] The method of claim 14, wherein said substrate is intrinsic or P-doped to a maximum concentration of 1E17 atm/cm^3 and said buried N-doped region are formed by ion implantation of an N-type dopant ion with a dose of 1E14 to 1E16 atm/cm^2.

[c24] The method of claim 14, wherein said buried N-doped region is formed by ion implantation of arsenic or phosphorous.

[c25] The method of claim 14, wherein steps (c) and (d) are independently performed using one or more plasma etch processes.

[c26] The method claim 14, further comprising:
forming an N-well or a P-well region in said substrate, said N-well or P-well partially bounded by said lateral trench; and
respectively forming the source and drain of an NFET or a PFET in said N-well or said P-well.

[c27] A semiconductor device comprising:
a semiconductor substrate having a top surface;
a first region of said substrate having a first N-well, a first P-well or both a first N-well and a first P-well extending into said semiconductor substrate from said top surface and bounded in a direction perpendicular to said top surface by a first vertical trench isolation extending perpendicular to said top surface,

the source and drain of a first NFET, a first PFET or both a first NFET and a first PFET formed respectively in said first P-well or said first N-well of said first region; and
a second region of said substrate having a second N-well, a second P-well or both a second N-well and a second P-well, a lateral trench isolation extending laterally in a direction parallel to said top surface into said second N-well, said second P-well or both said second N-well and said second P-well from a second vertical trench isolation, said second vertical trench isolation extending perpendicular to said top surface, the source and drain of a second NFET, a second PFET or both a second NFET and a second PFET formed respectively in said second P-well or said second N-well of said second region.

[c28] The semiconductor device of claim 27, wherein a vertical edge of said lateral trench isolation is aligned to an outer edge of a spacer formed on a sidewall of a gate electrode of said second NFET or second PFET, aligned to said sidewall of said gate electrode, aligned between said outer edge of said spacer and said sidewall of said gate or aligned between two opposite sides of said gate electrode.

[c29] The semiconductor device of claim 27, wherein said source and drain of said second NFET or second PFET are in contact with an upper lateral surface of said lateral trench isolation.

[c30] The semiconductor device of claim 27 further including a

buried oxide layer in said substrate.